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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/655,854

09/05/2003

Rafael Reif

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7590

12/20/2005

DALY, CROWLEY, MOFFORD & DURKEE, LLP
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EXAMINER

ANDUJAR, LEONARDO

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/655,854

Applicant(s)

REIF ET AL.

Examiner

Leonardo Andújar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8 and 10-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2,4-8 and 12-16 is/are allowed.
- 6) ☒ Claim(s) 17-41 is/are rejected.
- 7) ☒ Claim(s) 10 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 January 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on 10/27/2005 in response to the Office action mailed on 07/27/2005 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 2, 4-8 and 10-41.

Election/Restrictions

2. Applicant's election of species 2 in the reply filed on 05/11/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the third semiconductor structure according to claim 41 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary,

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the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 10 and 11 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In the instant case, claim 10 depends on cancelled claim 9.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 17-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato (US 4,939,568)

7. Regarding claim 17, Kato (e.g. fig. 3) show a multi layer integrated semiconductor structure, comprising:

A first device layer 1 including:

- First and second opposing surface
- A first semiconductor region (24, 25);
- A first dielectric material 29 disposed about the first doped semiconductor region, the dielectric material having at least a first via hole 6a;

A first conductive material 6a disposed in the via hole to provide a first conductive via having first and second opposing ends;

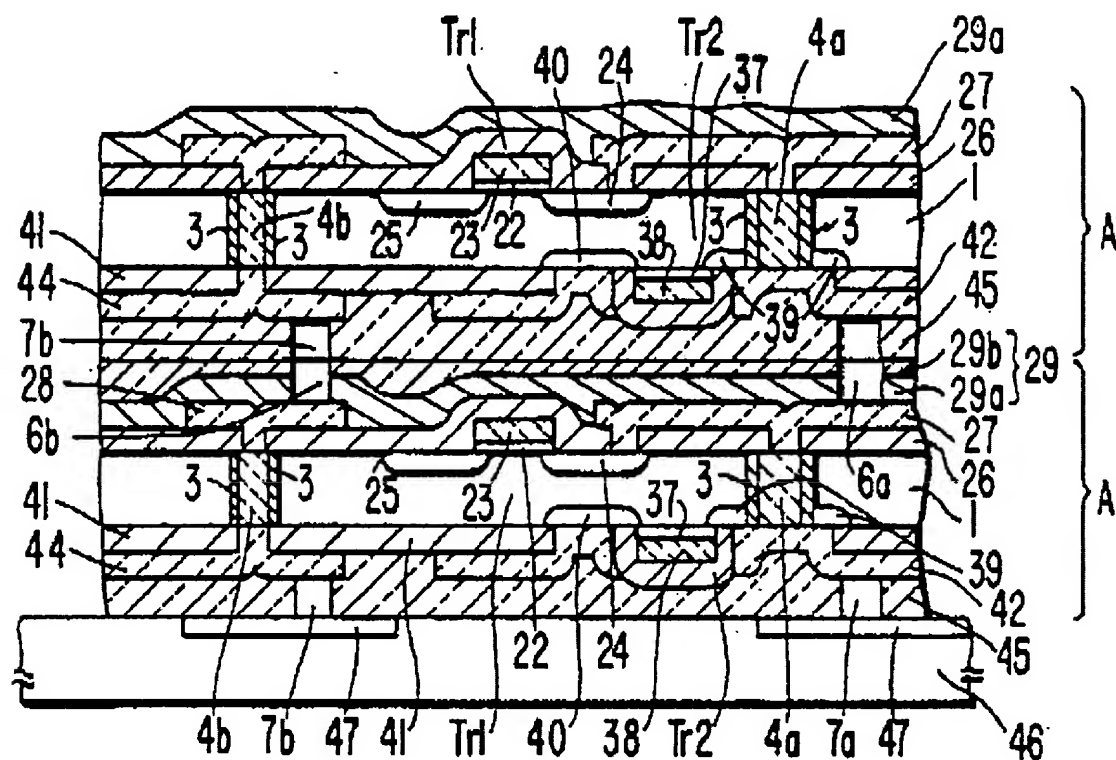
A second device layer 1 having first and second opposing surfaces including:

- At least a second doped semiconductor region (24, 25) and including a second via hole 4a; a second conductive material 4a disposed therein to provide a second conductive via having first and second ends;

A first interface "7a" (not labeled in the in figure 3 but located between 6a and 45) disposed between a first one of the first and second opposing surfaces of the first device layer and a first one of the first and second opposing surfaces of the second device layer such that the first interface secures together the first and second device layers and also electrically couples the first device layer to the second device layer wherein the conductive interface and the first and second conductive vias forms at least

a portion of an electrical communication path between the first device layer and the second device layer.

FIG. 3



8. Regarding claim 18, Kato shows a first conductive interconnect element 27 disposed in the first layer with a first portion of the first conductive via electrically coupled to at least a portion of the first conductive interconnect element and a second portion of the first conductive interconnect element coupled to the first doped semiconductor region.
9. Regarding claim 19, Kato shows that the first conductive via couples the first conductive interconnect element to the first conductive interface.

10. Regarding claim 20, Kato shows that the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and is coupled to the second doped semiconductor region.

11. Regarding claim 21, Kato shows a third conductive via 4a coupled to the second doped semiconductor region.

12. Regarding claim 22, Kato shows a second conductive interface 7a disposed on the second one of the first and second opposing surfaces of the second device layer and wherein the third conductive via is provided having a first end coupled to the second doped semiconductor region and a second end coupled to the second conductive interface.

13. Regarding claim 23, Kato shows that the second conductive via is formed on the first one of the first and second opposing surface of the second device layer and wherein the second device layer comprises a first conductive interconnect 27.

14. Regarding claim 24, Kato shows that the second conductive via is provided having a first end coupled to the conductive interconnect 27 and a second end coupled to the first conductive interface.

15. Regarding claim 25, Kato shows that the first conductive via is coupled to at least the first doped semiconductor region.

16. Regarding claim 26, Kato shows that the first conductive via is provided having a first end coupled to at least the first doped semiconductor region and a second end coupled to the first conductive interface.

17. Regarding claim 27, Kato shows that the first interface corresponds to a first conductor interface region (right side). Also, a second interface region (left side) is disposed between the first one of the first and second device layers with the second interface region provided from a non-conductive material 29b.

18. Regarding claim 28, Kato shows that the first conductive interface region is provided from a conductive bonding material (e.g. fig. 4f, col. 5/ll. 51).

19. Regarding claim 29, Kato shows a second conductive interconnect element 27 disposed in the second device layer with a portion of the second conductive interconnect element coupled to the second conductive via and wherein the first conductive via, the first conductive interface and the second conductive via provide a direct vertical electrical connection between the first conductive interconnect element and the second conductive interconnect element.

20. Regarding claim 30, Kato shows that the first device layer is constructed and arranged to operate using at least one of electronic components (abstract).

21. Regarding claim 31, Kato shows that the second device layer is constructed and arranged to operate using at least one of electronic components (abstract).

22. Regarding claim 32, Kato shows that the first device layer includes a transistor.

23. Regarding claim 33, Kato shows that the second device layer includes a transistor.

24. Regarding claims 34 and 35, Kato shows that the first and second device layers includes a die element (transistor) located on a wafer (col. 7/lls. 43-35).

25. Regarding claim 36, Kato shows that the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.

26. Regarding claim 37, Kato shows that the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area is substantially equivalent to the first predetermined surface area.

27. Regarding claim 38, Kato shows a first conductive interconnect element 27 having a first portion coupled to the first doped semiconductor region, and a second portion coupled to a first end of the first conductive via.

28. Regarding claim 39, Kato shows a second conductive interconnect element 27 having a first portion coupled to the second doped semiconductor region and a second portion coupled to a first end of the second conductive via with the second end of the first conductive via and the second end of the second conductive via each coupled to the first interface.

29. Regarding claim 40, Kato (e.g. fig. 3) shows a multi layer integrated semiconductor structure, comprising: a first semiconductor wafer 1 including a plurality of semiconductor structures (transistors) each of which includes a first plurality of semiconductor elements (24, 25, 27); a second semiconductor wafer 1 including a second plurality of semiconductor structures (transistors) each of which includes a second plurality of semiconductor elements (24, 25, 27); and at least a first conductive

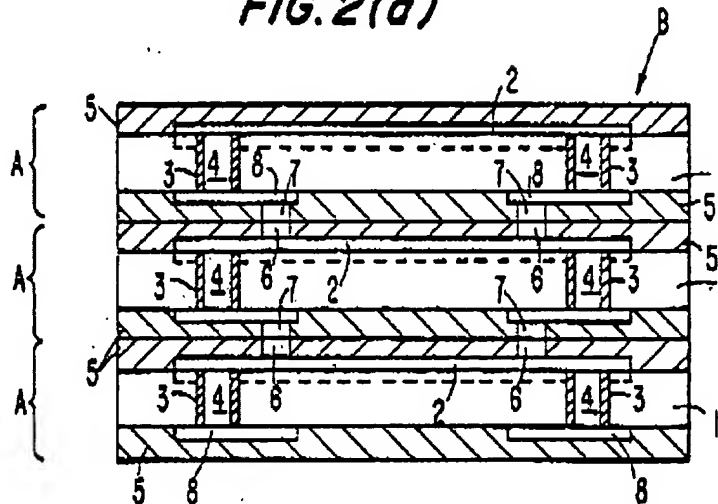
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bonding interface segment 7b disposed between the first and second semiconductor wafers; the first conductive bonding interface segment disposed over at least a first one of the plurality of semiconductor structures of the first semiconductor wafer and being in an electrical communication relationship with at least a first one of the first plurality of the semiconductor elements of the first semiconductor structure and; first one of the plurality of semiconductor elements of the second semiconductor structure of the second semiconductor wafer where the first conductive bonding interface segment permits at least the first semiconductor element of the first semiconductor structure to communicate with at least the second semiconductor element of the second semiconductor structure.

30. Regarding claim 41, Kato shows (e.g. figs. 2a and 3) shows a multi layer semiconductor structure, comprising: at least a first semiconductor structure 1 including a first plurality of conductive elements 4; at least a second semiconductor structure 1 including a second plurality of conductive elements 4; a first plurality of conductive bonding interface segments 7 disposed between the first and second semiconductor structures with each of the plurality of conductive bonding interface segments being in an electrical communication relationship with one or more of the conductive elements of the first semiconductor structure and one or more of the conductive elements of the second semiconductor structure; at least a third semiconductor structure 1 including a third plurality of conductive elements 4 and a second plurality of conductive bonding interface 7 disposed between the second and third semiconductor structures with each of the second plurality of conductive bonding interface segments being in electrical

communication relationship with one or more of the conductive elements of the second semiconductor structure and one or more of the conductive elements of the third semiconductor structure.

FIG. 2(a)



Allowable Subject Matter

31. Claims 1, 2, 4-8 and 12-16 are allowed.

Response to Arguments

32. Applicant's arguments filed 10/27/2005 with respect to claims 17-41 have been fully considered but they are not persuasive. In response to applicant arguments directed to the drawing objections, the examiner respectfully noted that drawings must show every feature of the invention specified in the claims (emphasis added see 37 CFR 1.83(a)). In this case, the third semiconductor structure according to claim 41 must be shown. The examiner respectfully disagrees that this limitation does not admit illustration. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

33. Applicant argues that Kato does not describe an interface disposed between a first surface of the first device layer and a first surface of a second device layer because the interface is disposed is part of the device. Nevertheless, the claim specified that the interface is between the first device layer (emphasis added) and second device layer. In this case, the layer 45 that contains the interface is not part of the first and/or second device layer. Therefore, the interface "7a" disclosed by Kato is between the first surface of the first device layer and a first surface of a second device layer.

34. Applicant argues that nothing in Kato reference suggests that the Kato interface terminal 7b could function as a conductive bonding interface. Nevertheless, Kato shows that the interfaces 7b are part of and electrical interconnection and are used as testing pad therefore it has to be at least electrically conductive. Also, the interfaces can be labeled as bonding interfaces since there have been bonded by thermocompression and they are part of the bonding layer 49 (col. 4/10-12 & col. 7/lls. 27-28). Although the applicant uses terms different to those of Kato to label the claimed invention, this does not result in any structural difference between the claimed invention and the prior art. The use of different terminology to describe the plurality of elements that constitute an integrated circuit as this is just a writing style and the way in which a structural limitation is expressed does not affect the configuration of the described elements.

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

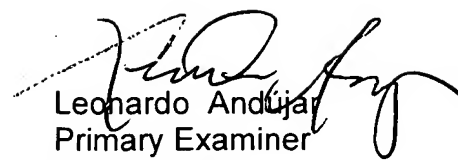
37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, appearing to read 'Leonardo Andujar', is written over the printed name and title.

Leonardo Andujar
Primary Examiner
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